



Chathil Rajamanthre Electrical Engineering Student

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TECHNICAL SKILLS

Languages — SystemVerilog, VHDL, C, ARMv7/Assembly, Python, Bash/Shell scripting

Verification & EDA Tools — Cadence Virtuoso, Spectre, UVM, LTspice, Matlab, Quartus, ModelSim, Git, Altium, Linux

Laboratory — FPGA, MCU, Soldering, Function generator, Multimeter, Oscilloscope, Logic Analyzer, PCB Design

EDUCATION

Bachelor of Applied Science - Electrical Engineering (Co-op), Sep 2023 – May 2028 | Vancouver, BC

University of British Columbia, CGPA: 80.8%, Available for 16 months

Relevant courses: Analog CMOS Integrated Circuit Design, Digital Systems Design, Signals and Systems

TECHNICAL WORK EXPERIENCE

University of British Columbia, Undergraduate Teaching Assistant Jan 2025 – Present | Vancouver, BC

- Offered individualized support to students in **C** programming and **Arduino**-based microcontroller development
- Debugged student code and piloted exam questions for APSC 160: Intro to Computation in Engineering Design

UBC Bionics, Electrical Team Lead Sep 2023 – Present | Vancouver, BC

- **Leading** a 12-member engineering subteam within a multidisciplinary student design team to develop GRASP, a bionic arm, focusing on EMG signal acquisition, battery management, and haptic boards with firmware
- Supporting recruitment efforts through candidate interviews and talent development by **mentoring** team members
- Designing a custom 4-layer **mixed-signal** EMG acquisition **PCB** on **Altium** with a low-noise analog front end, including precision **amplification**, **filtering**, and an **SPI**-interfaced ADC, applying **layout** techniques to minimize noise coupling

Dialog Network Services, Radio Network Planning Intern Jul 2025 – Aug 2025 | Colombo, Sri Lanka

- Supported cellular base station deployment through drive tests with TEMS Investigation and indoor walk tests with G-NetTrack Pro to assess antenna performance and diagnose signal coverage issues
- Proposed antenna upgrades for high-density events, aligning solutions with technical requirements

RESEARCH EXPERIENCE

Directed Studies on ADC-based Transceiver Architectures Jan 2026 – Present

- Conducting a survey on current state-of-the-art high-speed wireline transceiver designs from ISSCC/JSSC
- Performing system-level simulations using **MATLAB** SERDES Toolbox and design of modules (Phase detector, Loop filter, Current-Starved Ring VCO) for an **integer-N charge pump PLL** using **Cadence** in **GPDK45**

PROJECTS

RISC-V RV32E 5-Stage Pipeline Processor  , *Personal Project* Feb 2026 – Present

- Designing a 5-stage pipelined RISC-V RV32E processor in **SystemVerilog** with a **UVM** environment covering RTL blocks
- Targeting open-source silicon tapeout using Sky130 following an **RTL-to-GDSII** flow

Two-stage 45nm CMOS Op-Amp Design with CMFB  , *UBC ELEC 401* Nov 2025 – Dec 2025

- Designed a two-stage **differential to single-ended operational amplifier** in **GPDK45** using **Cadence EDA tools** to meet design requirements, achieving 52dB gain, 618MHz unity gain frequency, 65° phase margin, 0.65V output swing, and 48.45V/μs slew rate under 375μW of power consumption
- Applied **Miller compensation** with series RC zero placement to meet stability and bandwidth requirements
- Implemented a **common-mode feedback loop** to regulate output common-mode voltage
- Performed **AC**, **transient** and **stability** analyses (Bode plots, step response, settling time and slew-rate characterization)

FPGA Digital Signal Processing  , *UBC CPEN 311* Jun 2025

- Designed a digital communication system to enable hardware/software co-design in **SystemVerilog** and **embedded C** with the Nios II processor on the DE1-SoC to generate and view real-time ASK, BPSK and FSK modulation
- Integrated a Direct Digital Synthesis carrier signal generator and a 5-bit LFSR to modulate carrier waves with proper **clock domain crossing** techniques, validated using **SignalTap**
- Synthesized FSK modulation using **embedded C** on the Nios II processor by generating interrupts using **Qsys** PIOs

Proxmox Homelab Server, Personal Project May 2025 – Jul 2025

- Built a Proxmox-based virtualization environment hosting multiple **Linux** containers and virtual machines
- Automated game server deployment and firewall TCP/UDP rules using **Bash scripts**
- Deployed a Samba file server with a Tailscale VPN for secure remote file sharing across devices

Simple FPGA iPod, UBC CPEN 311 May 2025

- Implemented multiple **glitchless FSMs** and a configurable clock divider to read from flash memory and control audio playback including real-time speed adjustments via a PS/2 keyboard
- Designed a 2-stage **synchronizer** to safely transfer signals across asynchronous clock domains
- Performed real-time averaging of audio samples using assembly and an **interrupt service routine (ISR)** on an embedded processor (**PicoBlaze**) to create an audio strength meter